

WHAT IS CLAIMED IS:

1 1. Apparatus for deterring failure of a computing system;
2 said apparatus comprising:
3 an exclusively hardware network of components, having
4 substantially no software;
5 terminals of the network for connection to such system;
6 and
7 fabrication-preprogrammed hardware circuits of the net-
8 work for guarding such system from failure.

1 2. The apparatus of claim 1, particularly for use with such
2 system that is substantially exclusively made up of substan-
3 tially commercial, off-the-shelf components; and wherein:
4 at least one of the network terminals is connected to
5 receive at least one error signal generated by such system in
6 event of incipient failure of such system; and
7 at least one of the network terminals is connected to
8 provide at least one recovery signal to such system upon re-
9 ceipt of the error signal.

1 3. The apparatus of claim 2, wherein:
2 the circuits comprise portions fabrication-preprogrammed
3 to evaluate the at least one error signal to establish charac-
4 teristics of the at least one recovery signal.

1 4. The apparatus of claim 1, further comprising:
2 such computing system.

1 5. The apparatus of claim 1, wherein:
2 the circuits comprise portions for identifying failure of
3 any of the circuits and correcting for the identified failure.

1 6. The apparatus of claim 1, particularly for use with a
2 computing system that has at least one software subsystem for
3 conferring resistance to failure of the system; and wherein:
4 the circuits comprise substantially no portion that in-
5 terferes with such failure-resistance software subsystem.

1 7. The apparatus of claim 1, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one hardware subsystem for generating a response
5 of the system to failure; and wherein:

6 the circuits comprise portions for reacting to said re-
7 sponse of such hardware subsystem.

1 8. The apparatus of claim 1, particularly for use with a
2 computing system that has plural generally parallel computing
3 channels; and wherein:

4 the circuits comprise portions for comparing computatio-
5 nal results from such parallel channels.

1 9. The apparatus of claim 8, wherein:

2 the parallel channels of the computing system are of di-
3 verse design or origin.

1 10. The apparatus of claim 1, particularly for use with a
2 computing system that has plural processors; and wherein:
3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 11. The apparatus of claim 1, wherein:
2 the circuits comprise modules for collecting and respond-
3 ing to data received from at least one of the terminals, said
4 modules comprising:
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6 at least three data-collecting and -responding mod-
7 ules, and
8
9 processing sections for conferring among the modules
10 to determine whether any of the modules has
11 failed.

1 12. The apparatus of claim 1, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem
6 for receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis
8 and a corrective reaction between the response-generating sub-
9 system and the command-receiving subsystem.

1 13. Apparatus for deterring failure of a computing system;
2 said apparatus comprising:

3 a network of components having terminals for connection
4 to such system; and

5 circuits of the network for operating programs to guard
6 such system from failure;

7 the circuits comprising portions for identifying failure
8 of any of the circuits and correcting for the identified
9 failure.

1 14. The apparatus of claim 13, wherein:
2 the program-operating portions comprise a section that
3 corrects for the identified failure by taking a failed circuit
4 out of operation.

1 15. The apparatus of claim 14, wherein:
2 the program-operating portions comprise a section that
3 substitutes and powers up a spare circuit for a circuit taken
4 out of operation.

1 16. The apparatus of claim 13, further comprising:
2 such computing system.

1 17. The apparatus of claim 13, wherein:
2 the program-operating portions comprise at least three of
3 the circuits; and
4 failure is identified at least in part by majority vote
5 among the at least three circuits.

1 18. The apparatus of claim 13, particularly for use with a
2 computing system that has at least one software subsystem for
3 conferring resistance to failure of the system; and wherein:
4 the circuits comprise substantially no portion that in-
5 terferes with such failure-resistance software subsystem.

1 19. The apparatus of claim 13, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one hardware subsystem for generating a response
5 of the system to failure; and wherein:
6 the circuits comprise portions for reacting to said re-
7 sponse of such hardware subsystem.

1 20. The apparatus of claim 13, particularly for use with a
2 computing system that has plural generally parallel computing
3 channels; and wherein:
4 the circuits comprise portions for comparing computatio-
5 nal results from such parallel channels.

1 21. The apparatus of claim 20, wherein:

2 the parallel channels of the computing system are of di-
3 verse design or origin.

1 22. The apparatus of claim 13, particularly for use with a
2 computing system that has plural processors; and wherein:

3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 23. The apparatus of claim 13, wherein:

2 the circuits comprise modules for collecting and respond-
3 ing to data received from at least one of the terminals, said
4 modules comprising:

5
6 at least three data-collecting and -responding mod-
7 ules, and

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9 processing sections for conferring among the modules
10 to determine whether any of the modules has
11 failed.

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1 24. The apparatus of claim 13, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem
6 for receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis
8 and a corrective reaction between the response-generating sub-
9 system and the command-receiving subsystem.

1 25. Apparatus for deterring failure of a computing system
2 that has at least one software subsystem for conferring resis-
3 tance to failure of the system; said apparatus comprising:
4 a network of components having terminals for connection
5 to such system; and
6 circuits of the network for operating programs to guard
7 such system from failure;
8 the circuits comprising substantially no portion that in-
9 terferes with such failure-resistance software subsystem.

- 1 26. The apparatus of claim 25, further comprising:
 - 2 such computing system, including such at least one soft-
 - 3 ware subsystem.

- 1 27. The apparatus of claim 25, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one hardware subsystem for generating a response
5 of the system to failure; and wherein:
 - 6 the circuits comprise portions for reacting to said re-
 - 7 sponse of such hardware subsystem.

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1 28. The apparatus of claim 25, particularly for use with a
2 computing system that has plural generally parallel computing
3 channels; and wherein:

4 the circuits comprise portions for comparing computatio-
5 nal results from such parallel channels.

1 29. The apparatus of claim 28, wherein:

2 the parallel channels of the computing system are of di-
3 verse design or origin.

1 30. The apparatus of claim 25, particularly for use with a
2 computing system that has plural processors; and wherein:

3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 31. The apparatus of claim 25, wherein:

2 the circuits comprise modules for collecting and respond-
3 ing to data received from at least one of the terminals, said
4 modules comprising:

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6 at least three data-collecting and -responding mod-
7 ules, and

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9 processing sections for conferring among the modules
10 to determine whether any of the modules has
11 failed.

1 32. The apparatus of claim 25, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem
6 for receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis
8 and a corrective reaction between the response-generating sub-
9 system and the command-receiving subsystem.

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1 33. Apparatus for deterring failure of a computing system
2 that is substantially exclusively made of substantially com-
3 mercial, off-the-shelf components and that has at least one
4 hardware subsystem for generating a response of the system to
5 failure; said apparatus comprising:

6 a network of components having terminals for connection
7 to such system; and

8 circuits of the network for operating programs to guard
9 such system from failure;

10 the circuits comprising portions for reacting to said
11 response of such hardware subsystem.

1 34. The apparatus of claim 33, wherein:

2 the reacting portions comprise sections for evaluating
3 the hardware-subsystem response to establish characteristics
4 of at least one recovery signal.

1 35. The apparatus of claim 34, wherein:

2 the reacting portions comprise sections for applying the
3 at least one recovery signal to such system.

1 36. The apparatus of claim 33, further comprising:

2 such computing system, including such hardware subsystem.

1 37. The apparatus of claim 33, particularly for use with a
2 computing system that has plural generally parallel computing
3 channels; and wherein:

4 the circuits comprise portions for comparing computatio-
5 nal results from such parallel channels.

1 38. The apparatus of claim 37, wherein:

2 the parallel channels of the computing system are of di-
3 verse design or origin.

1 39. The apparatus of claim 33, particularly for use with a
2 computing system that has plural processors; and wherein:
3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 40. The apparatus of claim 33, wherein:
2 the circuits comprise modules for collecting and respond-
3 ing to data received from at least one of the terminals, said
4 modules comprising:
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6 at least three data-collecting and -responding mod-
7 ules, and
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9 processing sections for conferring among the modules
10 to determine whether any of the modules has
11 failed.

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1 41. The apparatus of claim 33, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem
6 for receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis
8 and a corrective reaction between the response-generating sub-
9 system and the command-receiving subsystem.

1 42. Apparatus for deterring failure of a computing system
2 that is distinct from the apparatus and that has plural gen-
3 erally parallel computing channels; said apparatus comprising:

4 a network of components having terminals for connection
5 to such system; and

6 circuits of the network for operating programs to guard
7 such system from failure;

8 the circuits comprising portions for comparing computa-
9 tional results from such parallel channels.

1 43. The apparatus of claim 42, wherein:

2 the parallel channels of the computing system are of di-
3 verse design or origin.

1 44. The apparatus of claim 42, wherein:

2 the comparing portions comprise at least one section for
3 analyzing discrepancies between the results from such parallel
4 channels.

1 45. The apparatus of claim 44, wherein:

2 the comparing portions further comprise at least one
3 section for imposing corrective action on such system in view
4 of the analyzed discrepancies.

1 46. The apparatus of claim 45, wherein:

2 the at least one discrepancy-analyzing section uses a
3 majority voting criterion for resolving discrepancies.

1 47. The apparatus of claim 42, further comprising:
2 such computing system.

1 48. The apparatus of claim 47, wherein:
2 the parallel channels of the computing system are of di-
3 verse design or origin.

1 49. The apparatus of claim 48, wherein:
2 the comparing portions comprise circuitry for performing
3 an algorithm to validate a match that is inexact.

1 50. The apparatus of claim 49, wherein:
2 the algorithm-performing circuitry employs a degree of
3 inexactness suited to a type of computation under comparison.

1 51. The apparatus of claim 49, wherein:
2 the algorithm-performing circuitry performs an algorithm
3 that selects a degree of inexactness based on type of computa-
4 tion under comparison.

1 52. The apparatus of claim 42, particularly for use with a
2 computing system that has plural processors; and wherein:
3 the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

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1 53. The apparatus of claim 42, wherein:

2 the circuits comprise modules for collecting and respond-
3 ing to data received from at least one of the terminals, said
4 modules comprising:

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6 at least three data-collecting and -responding mod-
7 ules, and

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9 processing sections for conferring among the modules
10 to determine whether any of the modules has
11 failed.

1 54. The apparatus of claim 42, particularly for use with a

2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem
6 for receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis
8 and a corrective reaction between the response-generating sub-
9 system and the command-receiving subsystem.

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1 55. Apparatus for deterring failure of a computing system
2 that has plural processors; said apparatus comprising:
3 a network of components having terminals for connection
4 to such system; and
5 circuits of the network for operating programs to guard
6 such system from failure;
7 the circuits comprising portions for identifying failure
8 of any of such processors and correcting for identified
9 failure.

1 56. The apparatus of claim 55, wherein:
2 the identifying portions comprise a section that corrects
3 for the identified failure by taking a failed processor out of
4 operation.

1 57. The apparatus of claim 56, wherein:
2 the section comprises parts for taking a processor out of
3 operation only in case of signals indicating that the proces-
4 sor has failed permanently.

1 58. The apparatus of claim 55, wherein:
2 the identifying portions comprise a section that substi-
3 tutes and powers up a spare circuit for a processor taken out
4 of operation.

1 59. The apparatus of claim 55, further comprising:
2 such computing system.

1 60. The apparatus of claim 55, wherein:
2 the circuits comprise modules for collecting and respond-
3 ing to data received from at least one of the terminals, said
4 modules comprising:

5
6 at least three data-collecting and -responding mod-
7 ules, and

8
9 processing sections for conferring among the modules
10 to determine whether any of the modules has
11 failed.

1 61. The apparatus of claim 55, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem
6 for receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis
8 and a corrective reaction between the response-generating sub-
9 system and the command-receiving subsystem.

1 62. Apparatus for deterring failure of a computing system;
2 said apparatus comprising:
3 a network of components having terminals for connection
4 to such system; and
5 circuits of the network for operating programs to guard
6 such system from failure;
7 the circuits comprising modules for collecting and re-
8 sponding to data received from at least one of the terminals,
9 said modules comprising:
10 at least three data-collecting and -responding mod-
11 ules, and
12 processing sections for conferring among the modules
13 to determine whether any of the modules has
14 failed.

1 63. The apparatus of claim 62, further comprising:
2 such computing system.

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1 64. The apparatus of claim 62, particularly for use with a
2 computing system that is substantially exclusively made of
3 substantially commercial, off-the-shelf components and that
4 has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem
6 for receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis
8 and a corrective reaction between the response-generating sub-
9 system and the command-receiving subsystem.

1 65. Apparatus for deterring failure of a computing system
2 that is substantially exclusively made of substantially com-
3 mercial, off-the-shelf components and that has at least one
4 subsystem for generating a response of the system to failure,
5 and that also has at least one subsystem for receiving recov-
6 ery commands; said apparatus comprising:

7 a network of components having terminals for connection
8 to such system between the response-generating subsystem and
9 the recovery-command-receiving subsystem; and

10 circuits of the network for operating programs to guard
11 such system from failure;

12 the circuits comprising portions for interposing analysis
13 and a corrective reaction between the response-generating sub-
14 system and the command-receiving subsystem.

1 66. The apparatus of claim 62, further comprising:
2 such computing system.